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EXAMINER	
BRINEY III, WALTER F	

ART UNIT	PAPER NUMBER
2644	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/605,953	FISCHER ET AL.	
	Examiner	Art Unit	
	Walter F Briney III	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

Claim 2 is objected to because of the following informalities: a period is missing at the end of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 18 recites the limitation **"wherein said fixed voltage is analog ground"** in lines 1 and 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-6, 9-11, 27-32, and 34-35 are rejected under 35 U.S.C. 102(a) as being anticipated by the prior art admitted by the applicant.

Claim 1 is limited to **a circuit for detecting whether a telecommunications line is off-hook**; the admitted prior art discloses detecting an off-hook state on a telecommunications line (page 3, lines 3-7). **Said telecommunication line comprising tip and ring signal lines**; the circuit is used with both tip and ring lines (page 3, lines 3-7). **Said circuit comprising: a voltage divider for coupling between said tip and ring lines and having a node at which is presented a scaled version of a voltage across said voltage divider**; the admitted prior art discloses a voltage divider (figure 1, element 17) with a node where a common (i.e. scaled) voltage appears (figure 1, element 22). **A transistor having a control terminal coupled to said node**; the admitted prior art discloses a transistor in an optical coupler (figure 1, element 28) with a base (i.e. control) coupled to the node through the comparator (figure 1, element 24) and the optical diode (figure 1, element 28). **First and second current flow terminals coupled between a voltage source and an output terminal**; the admitted prior art discloses a transistor coupled to ground (i.e. power source) and an output connected to a DSP (figure 1, element 25). **Whereby said output terminal bears a value that is indicative of the voltage across said tip and ring lines and thus whether said telecommunications line is off-hook**; the admitted prior art discloses that the output of the transistor is based on the output of a comparator (figure 1, element 24) which is based off of a node (figure 1, element 22) which is based off of whether a line is off-hook. Therefore, the admitted prior art discloses all limitations of the claim.

Claim 2 is limited to **the circuit of claim 1**, as covered by the admitted prior art, **wherein: said voltage divider comprises a first resistor having a first terminal for coupling to said tip line**; the admitted prior art discloses a resistor (figure 1, element 18) connected to TIP through a bridge rectifier (figure 1, element 12) and signal TIP'. **A second terminal coupled to said node**; the admitted prior art discloses the resistor connected to a node (figure 1, element 22). **A second resistor having a first terminal for coupling to said ring line and a second terminal coupled to said node**; the admitted prior art discloses a resistor (figure 1, element 20) connected to RING through a bridge rectifier (figure 1, element 20) and signal RING', and connected to the node (figure 1, element 22). Therefore, the admitted prior art discloses all limitations of the claim.

Claim 3 is limited to **the circuit of claim 2**, as covered by the admitted prior art, **further comprising: an analog to digital converter having an analog input and a digital output**; the admitted prior art discloses a comparator with an analog input from the voltage divider and a bistable output (i.e. digital) (figure 1, elements 24 and 28). **Said analog input coupled to said output terminal wherein said analog input is based to a voltage different than a voltage of said voltage source**; the admitted prior art discloses an input received from the voltage divider (i.e. different than voltage source) (figure 1, element 22) and coupled to the output of the transistor through the comparator, optical diode, and the base of the transistor. Therefore, the admitted prior art discloses all limitations of the claim.

Claim 4 is limited to **the circuit of claim 3**, as covered by the admitted prior art, **wherein said voltage of said voltage source is ground**; the admitted prior art discloses hooking one side of the transistor (figure 1, element 28) to ground. Therefore, the admitted prior art discloses all limitations of the claim.

Claim 5 is limited to **the circuit of claim 3**, as covered by the admitted prior art, **further comprising: a processor coupled to said digital output of said analog to digital converter**; the admitted prior art discloses a DSP (i.e. processor) (figure 1, element 25) connected to the optical coupler's output (i.e. digital output). **Said processor adapted to determine whether said telecommunication line is off-hook based on a signal on said digital output of said analog to digital converter**; the processor acts based on the hook state (i.e. determines) of the line based on the input from the comparator (i.e. analog to digital converter) (page 4, lines 11-22). Therefore, the admitted prior art discloses all limitations of the claim.

Claim 6 is limited to **the apparatus of claim 3**, as covered by the admitted prior art, **wherein said analog-to-digital converter is a differential converter**; the admitted prior art discloses a converter (figure 1, element 24) comprised of a comparator that computes a difference (i.e. differential) and outputs a binary result (i.e. digital). **Comprising first and second analog input terminals**; the admitted prior art discloses an analog input (i.e. first) to the comparator (figure 1, element 24) and a second input from earth ground. **Said first analog input terminal coupled to tip**; the prior discloses the first input to the converter is from TIP via TIP'. **Said second analog input terminal coupled to ring**; the admitted prior art discloses a second input to RING through RING'

(i.e. earth ground). Therefore, the admitted prior art discloses all the limitations of the claim.

Claim 9 contains the essence of claim 5 as covered by the admitted prior art. Therefore, the admitted prior art has been shown to disclose all limitations of the claim with the exception of **wherein said processor is adapted to disable said first circuit responsive to said analog-to-digital converter receiving said second voltage and enable said first circuit responsive to said analog-to-digital converter receiving said first voltage**; the admitted prior art discloses that the DSP (i.e. processor) (figure 1, element 25) is programmed to disable the telecommunication apparatus from going off-hook when the voltage across tip and ring is less than 30 volts (i.e. second voltage), but is enabled when the voltage is greater than 30 volts (i.e. first voltage) (page 4, lines 3-14). **A first circuit for taking said apparatus off-hook so that said apparatus may receive or transmit information via said telecommunication link**; the admitted prior art discloses a DSP to disable the ability of the apparatus to go off-hook so inherently a circuit exists for taking the device off-hook to connect to a line for transmitting and receiving. Therefore, the admitted prior art discloses all limitations of the claim.

Claim 10 is essentially the same as claim 2 and is rejected for the same reasons.

Claim 11 is essentially the same as claim 6 and is rejected for the same reasons.

Claim 27 is limited to **a method for detecting whether a telecommunication line is off-hook without affecting the line impedance, said telecommunication line comprising tip and ring signal lines, said method comprising the steps of: (1) modulating a DC voltage that appears across said tip and ring lines**; the admitted

prior art discloses passing voltage between TIP and RING lines to a digital domain using voltage division, comparison, and isolation (i.e. modulating) (figure 1, PC Power Domain and page 3, lines 3-16). **(2) passing said modulated DC voltage through an electrical high voltage interface circuit**; the prior discloses comparator's output (i.e. modulated DC voltage) is passed through an optical coupler (i.e. high voltage interface) (figure 1, element 28). **(3) determining whether said telecommunication line is off-hook as a function of said modulated DC voltage**; the prior discloses using a DSP (figure 1, element 25 and page 4, lines 11-22) to determine hook-state based on the voltage comparator's output (i.e. modulated DC voltage). Therefore, the admitted prior art discloses all limitations of the claim.

Claim 28 is limited to **the method of claim 27**, as covered by the admitted prior art, **wherein step (1) comprises converting said DC voltage appearing across said tip and ring lines from analog to digital**; the admitted prior art discloses converting the voltage divider output to one of two states (i.e. converting from analog to digital) using the comparator (page 4, lines 3-11). Therefore, the admitted prior art discloses all limitations of the claim.

Claim 29 is limited to **the method of claim 28**, as covered by the admitted prior art, **further comprising the step of: (4) scaling said analog DC voltage appearing across said tip and ring lines before step (1)**; the admitted prior art discloses voltage dividing the tip and ring lines (figure 1, element 17 and page 3, lines 3-11). Therefore, the admitted prior art discloses all limitations of the claim.

Claim 30 is rejected for the same reasons as claim 29.

Claim 31 is limited to **the method of claim 27**, as covered by the admitted prior art, **wherein step (3) comprises comparing said modulated DC voltage to a reference value**; the voltage divided output (i.e. modulated DC value) is compared to a reference value (figure 1, element 26). Therefore, the admitted prior art discloses all limitations of the claim.

Claim 32 is limited to **the method of claim 31**, as covered by the admitted prior art, **wherein step (3) is performed by a digital signal processor**; the admitted prior art discloses passing the digital output to a digital signal processor that further determines the hook state (page 4, lines 11-22). Therefore, the admitted prior art makes obvious all limitations of the claim.

Claim 34 is limited to **the method of claim 29**, as covered by the admitted prior art, **further comprising the steps of (6) converting said DC voltage to a two state signal indicative of said DC voltage before step (1)**; the admitted prior art discloses converting the voltage divider output to a two-state signal based on its voltage using a comparator (page 4, lines 3-11). Therefore, the admitted prior art discloses all limitations of the claim.

Claim 35 is limited to **the method of claim 34**, as covered by the admitted prior art, **wherein step (6) comprises controlling a transistor to turn on or off responsive to said DC voltage appearing across said tip and ring lines**. The admitted prior art discloses that a transistor that is part of an optical coupler (figure 1, element 28) turns on or off based on the output of a comparator (figure 1, element 24

and page 4, lines 3-11). Therefore, the admitted prior art discloses all limitations of the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the admitted prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 12 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Scott (US Patent 6,160,885).

Claim 7 is limited to **the circuit of claim 6**; as covered by the admitted prior art. Therefore, the admitted prior art has been shown to disclose all limitations of the claim with the exception of **a first capacitor coupled between said tip line and said first analog input terminal of said analog to digital converter and a second capacitor coupled between said ring line and said second analog input terminal of said analog to digital converter**; Scott teaches to multiplex an A/D converter for the purpose of reducing required hardware interfaces (column 27, line 58-column 28, line 12). It would have been obvious to one of ordinary skill in the art at the time of the invention to multiplex the use of the A/D of the admitted prior art between the TIP and RING lines and the hook detection circuitry as taught by Scott for the purpose of reducing hardware interfaces. Scott also teaches a capacitive interface between TIP and RING lines and their inputs to a mux that feeds into an A/D (figure 18, element

1812) (figure 18, element 1703 and column 22, line 58-column 23, line 65) for the purpose of blocking high-voltage DC current into the A/D It would have been obvious to one of ordinary skill in the art at the time of the invention to use a capacitive interface between the TIP and RING lines of the admitted prior art as taught by Scott for the purpose of blocking high-voltage DC currents from reaching the A/D converter.

Claim 12 is essentially the same as claim 7 and is rejected for the same reasons.

Claim 33 is limited to **the method of claim 29**, as covered by the admitted prior art, **further comprising the step of (5) selectively enabling said DC voltage appearing across said tip and ring lines to be modulated**. Scott teaches to implement a multiplexer for the purpose of selecting between hook switch detection and tip and ring lines (i.e. selectively enabling modulation) for the purpose of eliminating a need for a separate hardware interface (column 27, line 58 through column 28, line 12). Therefore, it would have been obvious to implement a multiplexer at the input of the A/D converter of the admitted prior art as taught by Scott for the purpose of supplying means to connect tip and ring lines to the A/D converter thus eliminating the need for an extra hardware interface.

Claims 8 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Scott as applied to claims 7 and 12 above, respectively, and further in view of Yong (US Patent 5,255,094).

Claim 8 is limited to **the apparatus of claim 7**; as covered by the admitted prior art in view of Scott. The admitted prior art in view of Scott has been shown to disclose all limitations of the claim with the exception of **a diode having an anode coupled to**

said node and a cathode coupled to a control signal; Yong teaches to couple the anode of a diode to an amplifier (i.e. comparator of the admitted prior art) and a cathode to a transient protection circuit (i.e. control signal) (figure 2, element 42) for the purpose of providing a shunt for transients when power is first applied to a circuit (column 3, lines 28-40). It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the transient protection circuit of Yong to the input of the comparator of the admitted prior art for the purpose of protecting the input of the comparator to transients when power is suddenly applied to the comparator. **Said control signal having a first state which turns said diode on and drives said node to a voltage that turns said transistor off**; Yong teaches a power supply that is turned off (i.e. first state) causing the diode to turn on, where the voltage present at the input to the comparator (i.e. node) will be shunted so the comparator's output will be low causing the transistor in the optical coupler to turn off (column 3, line 41 through column 4, line 5). **A second state that turns said diode off whereby said node is driven to a voltage dictate by said voltage across said tip and ring lines**; Yong teaches a power supply that turns on (i.e. second state) that turns the diode off, where the voltage present at the input is determined by the voltage divider across it, whose voltage is determined by the TIP and RING lines (column 3, line 41 through column 4, line 5). Therefore, the admitted prior art in view of Scott and further in view of Yong makes obvious all limitations of the claim.

Claim 13 is essentially the same as claim 8 and is rejected for the same reasons.

Claim 14 is limited to **the apparatus of claim 13**, as covered by the admitted prior art in view of Scott and in further view of Yong, **wherein said control signal is normally in said first state and is switched to said second state just before said first circuit is to take said apparatus off-hook**; Yong teaches that the diode is on (i.e. in first state) when power is newly applied and switched off (i.e. in second state) before and after a transient (i.e. before off-hook) (column 3, line 41 through column 4, line 5). Therefore, the admitted prior art in view of Scott and further in view of Yong makes obvious all limitations of the claim.

Claim 15 rejected for the same reasons as claim 14.

Claim 16 is limited to **the apparatus of claim 15**, as covered by the admitted prior art in view of Scott and in further view of Yong, **further comprising: a full wave rectifier circuit coupled between said detection circuit and said tip and ring lines**; the admitted prior art discloses a full wave rectifier coupled between the hook detection circuitry and TIP and RING (figure 1, element 12). Therefore, the admitted prior art in view of Scott and further in view of Yong makes obvious all limitations of the claim.

Claim 17 is limited to **the apparatus of claim 15**, as covered by the admitted prior art in view of Scott and in further view of Yong, **wherein said first and second inputs of said analog-to-digital converter are biased to common mode voltage**; the admitted prior art discloses two inputs to the comparator, the output of the voltage divider and ground, (i.e. A/D converter) based on TIP and RING signals in a telephone system which are inherently biased to common mode voltage (figure 1). Therefore, the

admitted prior art in view of Scott and in further view of Yong makes obvious all limitations of the claim.

Claims 19-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Scott and in further view of Jamshidi (US Patent 5,646,558).

Claim 19 is limited to **a circuit for detecting whether a telecommunication line is off-hook, said telecommunication line comprising tip and ring signal lines**; the admitted prior art discloses a circuit for detecting hook status of tip and ring lines (page 3, lines 3-7). **Said circuit comprising: a voltage divider for coupling between said tip and ring lines**; the admitted prior art discloses a voltage divider (figure 1, element 17) between tip and ring through lines tip' and ring', respectively. **Having first and second nodes across which appears a scaled version of a voltage across said tip and ring lines**; the admitted prior art discloses a node between two resistors (figure 1, element 22) and ground. **A differential analog-to-digital converter having first and second analog input terminals and a digital output terminal**; the admitted prior art discloses an analog-to-digital converter comprising a comparator (i.e. differential) and optical coupler (figure 1, elements 24 and 28) with an input from the first node and an input from ground (i.e. second node) with a bistable output. Therefore, the admitted prior art has been shown to disclose all limitations of the claim with the exception of **a signal line for selectively enabling said circuit when said signal is in a first state and disabling said circuit when said signal is in a second state; a first transistor having a control terminal coupled to said signal line and first and**

second current flow terminals coupled between said first node and said first input terminal of said analog-to-digital converter; whereby, when said signal line is in said first state, said analog-to-digital converter receives a scaled version of the voltage across said tip and ring lines and, when said signal line is in said second state, said analog-to-digital converter receives no signal from said voltage divider; Scott teaches to implement a multiplexer for the purpose of alternatively selecting between DC hook switch detection (i.e. voltage divider of the admitted prior art with first and second node) and AC tip and ring lines for the purpose of eliminating a need for a separate caller-id interface (column 27, line 58-column 28, line 12). Therefore, it would have been obvious to implement a multiplexer at the input of the A/D converter of the admitted prior art as taught by Scott for the purpose of supplying means to connect tip and ring lines to the A/D converter thus eliminating the need for an extra hardware interface. Jamshidi teaches to build a multiplexer using pass gate logic that passes a transistor's input (i.e. first node) to its output (i.e. input of A/D) (i.e. enables analog-to-digital converter to receive a scaled version of the voltage across said tip and ring lines) when a control signal (i.e. signal line for selectively enabling) is in a first state and blocks the input of a transistor from reaching its output (i.e. disabling the analog-to-digital input from the voltage divider so no signal is received) when the control signal is in a second state (figure 7 and column 5, line 27 through column 6, lines 22) where the size of a single transistor pass gate saves on area (column 2, lines 5-15). It would have been obvious at the time of the invention to use pass gate multiplexers in the multiplexing arrangement of the admitted prior art in view of Scott for the purpose of

saving area. **A second transistor having a control terminal coupled to said signal line and first and second current flow terminals coupled between said second node and said second input terminal of said analog-to-digital converter**; the admitted prior art teaches connecting two lines from the voltage divider to the input of the A/D (i.e. first node and second node), and using the pass-gate architecture of Jamshidi two transistors (i.e. first and second transistor) would inherently be needed for blocking and enabling both lines of the hook state detection circuitry. Therefore, the admitted prior art in view of Scott and in further view of Jamshidi makes obvious all limitations of the claim.

Claim 20 is essentially the same as claim 2 and is rejected for the same reasons.

Claim 21 is limited to **the circuit of claim 20**, as covered by the admitted prior art in view of Scott and in further view of Jamshidi, **further comprising a diode coupled between said second node and said ring line**; the admitted prior art discloses a diode as part of a bridge rectifier between ground (i.e. second node) and RING via RING'. Therefore, the admitted prior art in view of Scott and in further view of Jamshidi makes obvious all limitations of the claim.

Claim 22 is essentially the same as claim 5 and is rejected for the same reasons.

Claim 23 contains the essence of claim 19 as covered by the admitted prior art in view of Scott and in further view of Jamshidi. Therefore, the admitted prior art in view of Scott and in further view of Jamshidi has been shown to make obvious all limitations of the claim with the exception of **a processor**; the admitted prior art discloses the use of a DSP (figure 1, element 25). **Said processor is adapted to disable said first circuit**

responsive to said analog-to-digital converter receiving said second voltage and enable said first circuit responsive to said analog-to-digital converter receiving said first voltage; the admitted prior art discloses that the DSP (i.e. processor) (figure 1, element 25) is programmed to disable the telecommunication apparatus from going off-hook when the voltage across tip and ring is less than 30 volts (i.e. second voltage), but is enabled when the voltage is greater than 30 volts (i.e. second voltage) (page 4, lines 3-14). **A first circuit for taking said apparatus off-hook so that said apparatus may receive or transmit information via said telecommunication link;** the admitted prior art discloses a DSP to disable the ability of the apparatus to go off-hook so inherently a circuit exists for taking the device off-hook to connect to a line (i.e. to transmit or receive). Therefore, the admitted prior art in view of Scott and in further view of Jamshidi makes obvious all limitations of the claim.

Claims 24-26 are essentially the same as claims 20-22, respectively, and are rejected for the same reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F Briney III whose telephone number is 703-305-0347. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W Isen can be reached on 703-305-4386. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4700.

WFB
10/17/03

XU MEI
PRIMARY EXAMINER